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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/612,544	07/01/2003	Thomas E. Pearson	42P13560D	3569

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EXAMINER	
GRAYBILL, DAVID E	
ART UNIT	PAPER NUMBER
2822	

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/612,544	PEARSON ET AL.	
	Examiner	Art Unit	
	David E Graybill	2827	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 August 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 July 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7-1-3,1-9-4*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 7, 25, 30 and 31 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

There is insufficient antecedent basis for the following:

Claim 7, "said grooves";

Claim 13, "the conductive coating";

Claim 25, "the conductive material," and "the conductive column";

Claim 30, "each of the conductive columns."

Claims 7, 13, 25, 30 and 31 have not been rejected over the prior art because, in light of the 35 U.S.C. 112 rejection supra, there is a great deal of confusion and uncertainty as to the proper interpretation of the limitations of the claims; hence, it would not be proper to reject the claims on the basis of prior art. As stated in In re Steele, 305 F.2d 859, 134 USPQ 292 (CCPA 1962), a rejection should not be based on considerable speculation about the meaning of terms employed in a claim or assumptions that must be made as to the scope of the claims. Also see In re Wilson, 424 F.2d 1382, 165 USPQ 494 (CCPA 1970) (if no reasonably definite meaning can be

ascribed to certain claim language, the claim is indefinite, not obvious). See also MPEP 2143.03 and 2173.06.

In the rejections infra, generally, reference labels are recited only for the first recitation of identical claim elements.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 15, 16, 18-20, 23, 24, 26, 29 and 32 are rejected under 35 U.S.C. 102(e) as being anticipated by Okada (6534726).

At column 9, line 5 to column 10, line 2; and column 11, line 1 to column 14, line 41, Okada discloses the following:

A method of manufacturing an interposer, the method comprising: creating a plurality of via holes 22/52,65 through a circuit board substrate 21 from a first surface of the substrate to a second surface of the substrate; and creating a solid conductive column 57 through each of the via holes, the

conductive column forming an electrical path from the first surface to the second surface; coating the first surface and the second surface with a conductive material 55, 56; forming grooves 53 in the first surface and the second surface of the substrate between the via holes; coupling the interposer between an electronic component package 12 and a circuit board 5; wherein the electronic component package includes a semiconductor die and the circuit board is a motherboard.

A method of manufacturing an interposer, the method comprising: creating a plurality of via holes through a circuit board substrate from a first surface of the substrate to a second surface of the substrate; creating a conductive path 54 through each of the via holes from the first surface to the second surface; and forming a plurality grooves in the first surface and the second surface of the substrate between the via holes; wherein said forming a plurality grooves comprises: forming a first plurality of grooves (any two grooves) in the first surface of the substrate; forming a second plurality of grooves (any two grooves other than the first plurality) in the first surface of the substrate, perpendicular to the first plurality of grooves; forming a third plurality of grooves in the second surface of the substrate (the first plurality of grooves); forming a fourth plurality of grooves (the second plurality of grooves) in the second surface of the substrate,

perpendicular to the third plurality of grooves; wherein said creating a conductive path through each of the via holes comprises forming a thin conductive layer on a surface of each of the via holes; wherein said creating a conductive path through each of the via holes comprises forming a solid conductive column 57 through each of the via holes; coupling the interposer between an electronic component package and a circuit board.

To further clarify the disclosure of forming a second plurality of grooves perpendicular to the first plurality of grooves; and forming a fourth plurality of grooves perpendicular to the third plurality of grooves, it is noted that the grooves are three dimensional; therefore, each groove extends in a dimension perpendicular to every other groove.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the

contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claims 1, 2, 6, 8, 12, 14, 17 and 27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okada (6534726).

As cited supra, Okada discloses the following:

A method comprising: creating a plurality of rows (illustrated in FIG.9 in the plane of the paper as the three parallel vertical rows defining the vertical sides of the four substrate members 11) of via holes 22/52,65 through a circuit board substrate 21 from a first surface 51A of the substrate to a second surface 51B of the substrate; forming a conductive layer 55, 56 on the first surface and on the second surface; forming a conductive path 54 through each of the via holes from the first surface to the second surface; and severing the substrate through each row of via holes and between each row of via holes along a coordinate axis "the line passing trough [sic] the centers of the solder accommodation holes," to produce a plurality of substrate members 11/51; coupling at least one of the substrate members between an electronic component package 12 and a circuit board 5; forming

a plurality of elongate grooves in the first surface and in the second surface of the substrate, prior to said severing.

A method of manufacturing an interposer, the method comprising: creating a plurality of rows of via holes through a circuit board substrate from a first surface of the substrate to a second surface of the substrate, the first surface and the second surface being coated with a conductive material 55, 56; forming a conductive layer 54 in each of the via holes to provide a conduction path through each of the via holes from the conductive material on the first surface to the conductive material on the second surface; selectively removing "etching" some of the conductive material from the first surface to form a plurality of traces 55 on the first surface and the second surface, each trace in electrical contact with the conductive layer in at least one of the via holes; and severing the substrate to produce a plurality of individual substrate members, by cutting the substrate through the middle of the via holes in each row of via holes and between each row of via holes along a particular axis "the line passing trough [sic] the centers of the solder accommodation holes"; forming grooves in the first surface and the second surface of the substrate between the via holes; coupling at least one of the individual substrate members between an electronic component package and a circuit board; selectively removing some of the conductive material from

the first surface to form a plurality of traces on the first surface and the second surface, each trace in electrical contact with the conductive column of one of the via holes; severing the substrate to produce a plurality of beams 11/51, by cutting the substrate through the middle of the via holes in each row of via holes and between each row of via holes along a particular axis "the line passing trough [sic] the centers of the solder accommodation holes."

To further clarify, Okada discloses beams 11/51 because Okada discloses principal horizontal supporting members 11/51.

However, Okada does not appear to explicitly disclose elongate substrate members or elongate beams.

Notwithstanding, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose this particular shape because applicant has not disclosed that, in view of the applied prior art, the shape is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical, and it appears prima facie that the process would possess utility using another shape. Indeed, it has been held that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected

result, or are otherwise critical. See, for example, In re Rose, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); In re Rinehart, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); Gardner v. TEC Systems, Inc., 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); In re Dailey, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

Also, Okada does not appear to explicitly disclose removing some of the conductive material from the second surface to form a plurality of traces on the second surface.

Nonetheless, as set forth supra, Okada discloses forming a plurality of traces 56 on the second surface, and further discloses removing "etching" some of the conductive material from the first surface to form a plurality of traces 55 on the first surface. Moreover, it would have been obvious to remove the conductive material from the second surface by "etching" to form the plurality of traces on the second surface.

Claims 3-5 and 9-11, 21, 22 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Okada as applied to claims 1 and 8, 15 and 23 supra, and further in combination with Lin (5222014). Okada does not appear to explicitly disclose affixing two or more of the elongate substrate members together to form an interposer; wherein said affixing comprises affixing two or more of the elongate substrate members

together to form an interposer configured with an array of via holes; affixing two or more of the plurality of individual substrate members together to form an interposer as a substantially planar array; wherein each of the conductive columns has a composition of tin (Sn) and lead (Pb); wherein the composition comprises at least 81% lead (Pb); affixing two or more of the plurality of beams together in an array configuration to form the interposer.

Regardless, at column 3, lines 1-26; column 3, line 58 to column 2, line 49; column 5, lines 29-31; and column 6, lines 22-59, Lin discloses affixing two or more of the substrate members 12, 20 together to form an interposer; wherein said affixing comprises affixing two or more of the substrate members together to form an interposer configured with an array of via holes 24; affixing two or more of the plurality of individual substrate members together to form an interposer as a substantially planar array; wherein each of the conductive columns has a composition of tin (Sn) and lead (Pb); wherein the composition comprises at least 81% lead (Pb); affixing two or more of the plurality of beams 12/20 together in an array configuration to form the interposer.

In addition, it would have been obvious to combine this disclosure of Lin with the disclosure of Okada because it would provide a densely packed device.

To further clarify the disclosure wherein the composition comprises at least 81% lead, Lin discloses, "This solder, for example, may be of an 80/20 Pb/Sn composition or any other workable solder alloy composition," and a composition comprising at least 81% lead is a workable solder alloy composition.

In any case, Lin discloses that lead concentration is a result-effective variable. Moreover, it would have been an obvious matter of design choice bounded by well known manufacturing constraints and ascertainable by routine experimentation and optimization to choose the particular claimed lead concentration limitation because applicant has not disclosed that, in view of the applied prior art, the limitation is for a particular unobvious purpose, produces an unexpected result, or is otherwise critical, and it appears prima facie that the process would possess utility using another concentration. Indeed, it has been held that optimization of range limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See MPEP 2144.05(II): "Generally, differences in concentration or temperature will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such concentration or temperature is critical. '[W]here the general conditions of a

claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation.'" In re Aller, 220 F.2d 454, 105 USPQ 233, 235 (CCPA 1955). See also In re Hoeschele, 406 F.2d 1403, 160 USPQ 809 (CCPA 1969), Merck & Co. Inc. v. Biocraft Laboratories Inc., 874 F.2d 804, 10 USPQ2d 1843 (Fed. Cir.), cert. denied, 493 U.S. 975 (1989), and In re Kulling, 897 F.2d 1147, 14 USPQ2d 1056 (Fed. Cir. 1990). As set forth in MPEP 2144.05(III), "Applicant can rebut a prima facie case of obviousness based on overlapping ranges by showing the criticality of the claimed range. 'The law is replete with cases in which the difference between the claimed invention and the prior art is some range or other variable within the claims. . . . In such a situation, the applicant must show that the particular range is critical, generally by showing that the claimed range achieves unexpected results relative to the prior art range.' In re Woodruff, 919 F.2d 1575, 16 USPQ2d 1934 (Fed. Cir. 1990). See MPEP § 716.02 - § 716.02(g) for a discussion of criticality and unexpected results."

The art made of record and not applied to the rejection is considered pertinent to applicant's disclosure. It is cited primarily to show inventions similar to the instant invention.

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Any telephone inquiry of a general nature or relating to the status (MPEP 203.08) of this application or proceeding should be directed to Group 2800 Head SAE Linda Hodge-Taylor whose telephone number is 571-272-1585.

Any telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.

The fax phone number for group 2800 is (703) 872-9306.

David E. Graybill
Primary Examiner
Art Unit 2827

D.G.
21-Aug-04